1 CLAIMS:

2 1. A method of forming silicon nitride on a silicon-oxide-
3 comprising material, comprising:
4 exposing the silicon-oxide-comprising material to activated nitrogen
5 species from a nitrogen-containing plasma to introduce nitrogen into an
6 upper portion of the material; the silicon-oxide-comprising material being
7 maintained at a temperature of less than or equal to 200°C during the
8 exposing;
9 thermally annealing the nitrogen within the material to bond at
10 least some of the nitrogen to silicon proximate the nitrogen; and
11 after the annealing, chemical vapor depositing silicon nitride on the
12 nitrogen-containing upper portion of the material.
13

14 2. The method of claim 1 wherein the silicon-oxide-comprising
15 material comprises silicon dioxide.
16

17 3. The method of claim 1 wherein the silicon-oxide-comprising
18 material consists essentially of silicon dioxide.
19

20 4. The method of claim 1 wherein the silicon-oxide-comprising
21 material is at least 10Å thick, and wherein substantially all of the
22 nitrogen is within the top 5Å of the silicon-oxide-comprising material.
23

5. The method of claim 1 wherein the silicon-oxide-comprising material is less than or equal to about 5Å thick, and wherein the chemical vapor deposited silicon is at least about 10Å thick.

6. The method of claim 1 wherein the silicon-oxide-comprising layer is less than or equal to about 10Å thick, and wherein the chemical vapor deposited silicon is at least about 30Å thick.

7. The method of claim 1 wherein the silicon-oxide-comprising material is less than or equal to about 10Å thick, wherein the thermally annealed nitrogen is only within the top half of the silicon-oxide-comprising material, and wherein the chemical vapor deposited silicon is at least about 30Å thick.

8. The method of claim 1 wherein the silicon-oxide-comprising material is maintained at a temperature of from 50°C to 200°C during the exposing.

9. The method of claim 1 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

10. The method of claim 1 wherein the plasma is maintained with a power of from about 500 watts to about 3000 watts during the exposing.

11. The method of claim 1 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is less than or equal to about 3 Torr during the exposing.

12. The method of claim 1 wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

13. The method of claim 1 wherein the exposing occurs for a time of less than or equal to about 1 minute.

14. The method of claim 1 wherein the exposing occurs for a time of from about 3 seconds to about 1 minute.

15. The method of claim 1 wherein the exposing occurs for a time of from about 10 seconds to about 15 seconds.

16. The method of claim 1 wherein the annealing comprises rapid thermal processing at a ramp rate of at least about 50°C/sec to a temperature of less than 1000°C, with such temperature being maintained for at least about 30 seconds.

17. The method of claim 1 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

18. A method of forming a transistor device, comprising:

forming a silicon-oxide-comprising layer over a substrate;

exposing the silicon-oxide-comprising layer to activated nitrogen species from a nitrogen-containing plasma to introduce nitrogen into an upper portion of the layer;

thermally annealing the nitrogen within the layer to bond at least some of the nitrogen to silicon proximate the nitrogen;

after the annealing, chemical vapor depositing silicon nitride on the nitrogen-containing upper portion of the layer;

forming at least one conductive gate layer over the silicon nitride, the gate layer defining a channel region in the substrate beneath the silicon nitride; and

forming a pair of source/drain regions proximate the gate layer and gatedly connected to one another through the channel region.

19. The method of claim 18 wherein the silicon-oxide-comprising layer comprises silicon dioxide.

20. The method of claim 18 wherein the silicon-oxide-comprising layer consists essentially of silicon dioxide.

21. The method of claim 18 wherein the silicon-oxide-comprising layer is at least 10Å thick, and wherein substantially all of the nitrogen is within the top 5Å of the silicon-oxide-comprising layer.

22. The method of claim 18 wherein the silicon-oxide-comprising layer is less than or equal to about 5Å thick, and wherein the chemical vapor deposited silicon is at least about 10Å thick.

23. The method of claim 18 wherein the silicon-oxide-comprising layer is less than or equal to about 10Å thick, and wherein the chemical vapor deposited silicon is at least about 30Å thick.

24. The method of claim 18 wherein the silicon-oxide-comprising layer is less than or equal to about 10Å thick, wherein the thermally annealed nitrogen is only within the top half of the silicon-oxide-comprising layer, and wherein the chemical vapor deposited silicon is at least about 30Å thick.

25. The method of claim 18 wherein the substrate comprises a semiconductive material, and wherein the source/drain regions are formed as diffusion regions in the semiconductive material of the substrate.

26. The method of claim 18 wherein the silicon-oxide-comprising material consists essentially of silicon dioxide.

27. The method of claim 18 wherein the silicon-oxide-comprising material is maintained at a temperature of from 50°C to 200°C during the exposing.

28. The method of claim 18 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

29. The method of claim 18 wherein the plasma is maintained with a power of from about 500 watts to about 3000 watts during the exposing.

30. The method of claim 18 wherein the exposing occurs for a time of less than or equal to about 1 minute.

31. The method of claim 18 wherein the exposing occurs for a time of from about 3 seconds to about 1 minute.

32. The method of claim 18 wherein the exposing occurs for a time of from about 10 seconds to about 15 seconds.

33. The method of claim 18 wherein the annealing comprises rapid thermal processing at a ramp rate of at least about 50°C/sec to a temperature of less than 1000°C, with such temperature being maintained for at least about 30 seconds.

34. The method of claim 18 wherein the annealing comprises thermal processing at temperature of less than 1100°C for a time of at least 3 seconds.

35. A transistor device, comprising:

a silicon-oxide-comprising material over a substrate, the silicon-oxide-comprising material having a thickness of less than or equal to about 10Å;

a silicon-nitride-comprising material on the silicon-oxide-comprising layer, the silicon-nitride-comprising material having a thickness of at least 30Å, the silicon-nitride-comprising material being different than the silicon-oxide-comprising material;

at least one conductive gate layer on the silicon-nitride-comprising material, the gate layer defining a channel region in the substrate beneath the silicon-oxide-comprising material; and

a pair of source/drain regions proximate the gate layer and gatedly connected to one another through the channel region.

36. The device of claim 35 wherein the silicon-oxide-comprising material does not comprise nitrogen.

37. The device of claim 35 wherein the silicon-nitride-comprising material has a thickness of at least about 40Å.

38. The device of claim 35 wherein the silicon-oxide-comprising material has a thickness of 5Å or less.

39. The device of claim 35 wherein the silicon-nitride-comprising material has a thickness of at least about 40Å, and wherein the silicon-oxide-comprising material has a thickness of 5Å or less.

40. The device of claim 35 wherein the substrate comprises monocrystalline silicon, and wherein the source/drain regions are conductively doped diffusion regions within the substrate.